Multi Level Inverter with Dc Link Switches

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Abstract: - This paper presents a single phase 5 level inverter with dc link Switches using POD technique .The proposed multi level inverter is capable of generating 5 level output with less component count .This technique uses single carrier wave and two sine waves for pulse generation .The entire system is designed and implemented using MATLAB/Simulink .The inverter is connected to a R-load and performance are analysed.

Keywords: - 5level inverter, DC link switches, harmonics, R-load, POD technique, less component count, MLI, Electro magnetic interference (EMI)

I. INTRODUCTION

Now a days Multi level inverter are extensively used due to their increased power rating, reduced EMI , improving harmonic performance. Multi level inverters are switched at low switching frequency when compared to two level inverters, hence the switching losses are almost negligible .The multi level converter topology has drawn tremendous interest in the power industry since it can provide the high power required for high power applications.. To cope up with the problems associated with the two-level inverter, multi-level inverters (MLIs) are introduced

Multi level inverters are classified into 3 types

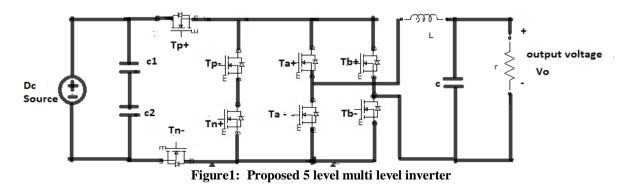
- Diode clamped multi level inverter
- Cascaded H bridge multi level inverter
- Flying capacitor type multi level inverter

The applications of multilevel inverter are reactive power compensation, variable speed drives etc. The topological structure of Multi level inverters should be capable of withstanding high input voltage for high power applications. A new multi level inverter is proposed which is capable of reducing problems faced by usage of conventional multi level inverters.

The advantages of proposed multi level inverter when compared with conventional Multi level inverter are : 1. Number of devices of the proposed multi-level inverter is fewer than that of the conventional multi-level inverters. Therefore, the proposed system is more reliable and cost competitive than the conventional two-level and multilevel inverters.2. Only one carrier signal is required to generate switching pulses to 8 switches used in proposed Multi level inverter [1].

II. PROPOSED 5 LEVEL MULTI LEVEL INVERTER

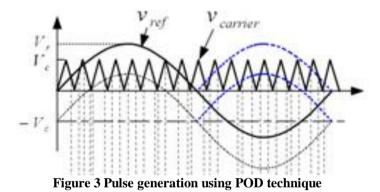
Figure 1 shows the proposed multi level inverter which is based on cascaded H bridge multi level inverter. In the proposed multi level inverter two dc link capacitors C1 and C2 and 8 dc link switches are used . Input supply to inverter is Vdc and voltage across each capacitor is Vdc/2. The output of the inverter is connected to LC filter in order to eliminate the harmonics. The switching sequence to generate 5 level output is shown in Figure2.



	SWITCHING CONDITION							
	TP+	TP-	Tn+	Tn-	Ta+	Tb-	Ta-	Tb +
Vdc	ON	OFF	OF	ON	ON	ON	OFF	OFF
Vdc/2	OFF	ON	OF	ON	ON	ON	OFF	OFF
Vdc/2	ON	OFF	ON	OFF	ON	ON	OFF	OFF
0	OFF	ON	ON	OFF	ON	ON	OFF	OFF
0	OFF	ON	ON	OFF	OFF	OFF	ON	ON
-vdc/2	OFF	ON	OFF	ON	OFF	OFF	ON	ON
-vdc/2	ON	OFF	ON	OFF	OFF	OFF	ON	ON
-vdc	ON	OFF	OFF	ON:	OFF	OFF	ON	ON

Figure 2 : Switching conditions of multi level inverter

II.a. PULSE GENERATION USING POD TECHNIQUE



POD stands for phase opposition and disposition technique. POD technique is used for pulse generation, this technique is used to turn on the switches used in proposed multilevel inverter. In the above figure single carrier wave and two sine waves are used for pulse generation. If sine wave 1 is greater than carrier wave then switches Tp+ is on else Tp- is on. If sine wave 2 is greater than carrier wave than switch Tn+ is on else switch Tn- is on. If sine wave 1 is positive then switches Ta+, Tb- are on and if sine wave is negative then switches Ta-, Tb+ is on .

III. SIMULATION

Simulation of proposed multi level inverter is carried out in MATLAB/Simulink .In Figure 4 Dc supply of 100 volts is given using batteries and 2 dc link capacitors are used and 8 MOSFET are used as dc link switches and output of multi level Inverter is connected to L,C filter to eliminate harmonics. The technique used for pulse generation is POD technique .Generally in order to turn on 8 switches 8 carrier signals are needed but using POD technique single carrier wave is used to generate switching pulses to 8 switches. Voltage measurement device is connected across each capacitor to measure the voltage across the capacitor.

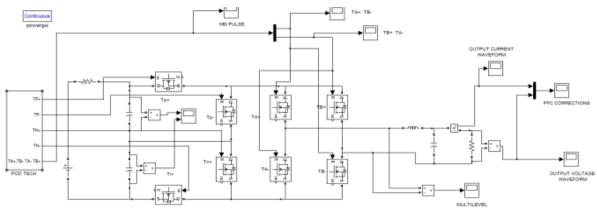


Figure 4 : Simulink diagram of main circuit

III.a SIMULINK DIAGRAM FOR PULSE GENERATION

For the simulation of 5 level inverter single carrier wave and two sine waves are generated as shown in Figure 5. Reference voltage for first sine wave is set as 1.7 volts and reference voltage for second sine wave is set as 0.8 volts. Both sine waves are operating at frequency at 50 hz. Time period for one carrier wave is set as 800 ms.

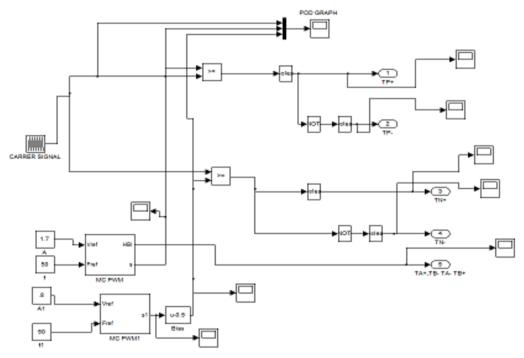


Figure 5 : Simulink diagram for pulse generation

PWM stands for pulse width modulation technique in which sine waves and carrier wave are compared for pulse generation. These pulses are used to turn on the Switches of multi level inverter. In case of pulse width modulated inverters input DC voltage is essentially constant in magnitude .The inverter must control the magnitude and frequency of ac output voltage. This can be achieved by PWM inverters. There are various techniques to pulse width modulate the inverter switches in order to shape the output voltage similar to sine wave used . In POD technique 2 sine waves and single carrier wave is used for pulse generation.. If sine wave is greater than Peak value of carrier wave then the technique is known as over modulation technique. A new multi level inverter is designed using PWM technique with less harmonics when compared to multi level inverter without using PWM technique. . PWM techniques commonly used are unipolar pulse width modulation technique.

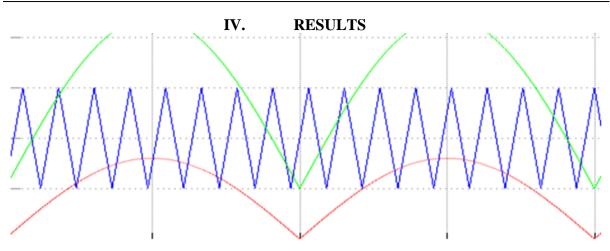


Figure 6 :Two sine waves and carrier wave for pulse generation

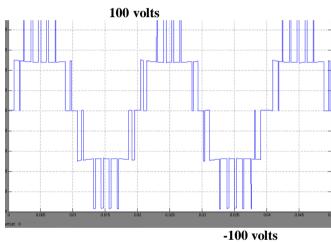
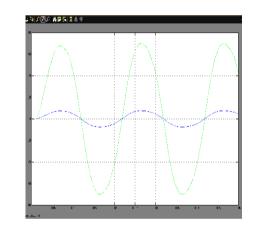
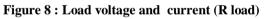


Figure 7 : Multi level inverter output





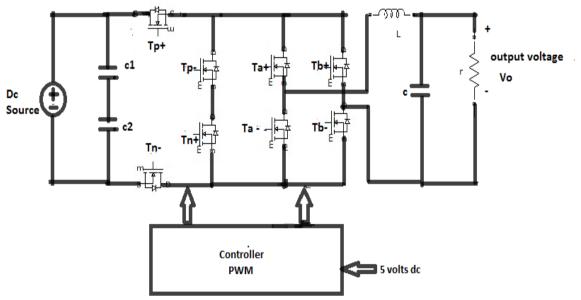


Figure 9: Single phase inverter system

IV.a. LOAD SPECIFICATIONS

Output power	:	250 W
Input voltage	:	100V
L	:	300 uh
С	:	150 uf

V. CONCLUSION

A new multi level inverter topology using POD technique is designed and the same is implemented in MATLAB/Simulink which is capable of producing 5 level output with less component count .No of dc supply sources used in proposed multi level inverter are less when compared to conventional Cascaded H bridge multi level inverter.

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REFERENCES

- [1] "Ho-Dong Sun1, Honnyong Cha1, Heung-Geun Kim1, Tae-Won Chun2, Eui-Cheol Nho" "Multi level inverter capable for power factor control with dc link switches "IEEE Trans. Ind. Electron vol.25,pp 400-408, March1991
- [2] H. Van der Broeck, "Analysis of the Harmonics in voltage-fed Inverter Drive caused by PWh4 schemes with Discontinuous Switching Operation," *EPE '91,Conference Proceedings*, vol. 3, pp. 261-266, 1991.
- [3] J. W. Kolar, H. Ertl, F. C. Zach, "Influence of the Modulation Method on the Conduction and SwitchingLosses of a PWM Converter System," *IEEE Trans. On Industry Applications*, Vol. 27, no. 6, pp. 1063 -1075, Nov./Dec. 1991.
- [4] Y. Ikeda, J. Itsumi, H. Funato, "The Power Loss of thevoltage-fed Inverter," in Proc. IEEE PESC'88, 1988, pp.
- [5] L. K. Mestha, P. D. Evans, "Analysis of on-state losses in PWM Inverters," *Proc. IEE-Elect.*
- [6] G. Grandi, C. Rossi, D. Ostojic, D. Casadei, "A New Multilevel Conversion Structure for Grid-Connected PV Applications", IEEE Trans. Ind. Electron., vol. 56, no. 11, pp. 4416-4426, Nov. 2009.
- [7]. "P. A. Dahono, Y. Sato, T. Kataoka, "Analysis of Conduction Losses in Inverters," *Proc. IEE-Elect. PowerApplicat.*, Vol. 142, no. 4, pp. 225-232, July 1995.